ABSTRACT OF THE DISCLOSURE:

A method and apparatus for real time capture of the desired failing chip cell diagnostic information from high speed testing of a semiconductor chip having built in self test functions and a fail trap register, and there is provided a programmable skip fail counter, and a hold and compare function circuit. The programmable skip counter is enabled for initialization to a "record first fail" mode, and then with non-zero values of the skip counter to a "record N^{th}+1 fail" mode. The "Record first fail" is considered the default or base function when the initial state of all registers is defined to be "0", and is obtained through scan initialization of the LSSD registers of the semiconductor chip. The diagnostic information for the chip is obtained by collecting data from scanning the circuits of said semiconductor chip for a failing cell for immediate scan-out off-chip at a level of assembly test, said level of assembly test being selected from a group consising of: an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology. The testing provides not only for the data collection of the first failing cell, but enables then skipping the collection of data up to a programmed amount to skip up to an "N^{th}" failing cell and recording the failure of the subsequent "N^{th}"+1 fail.